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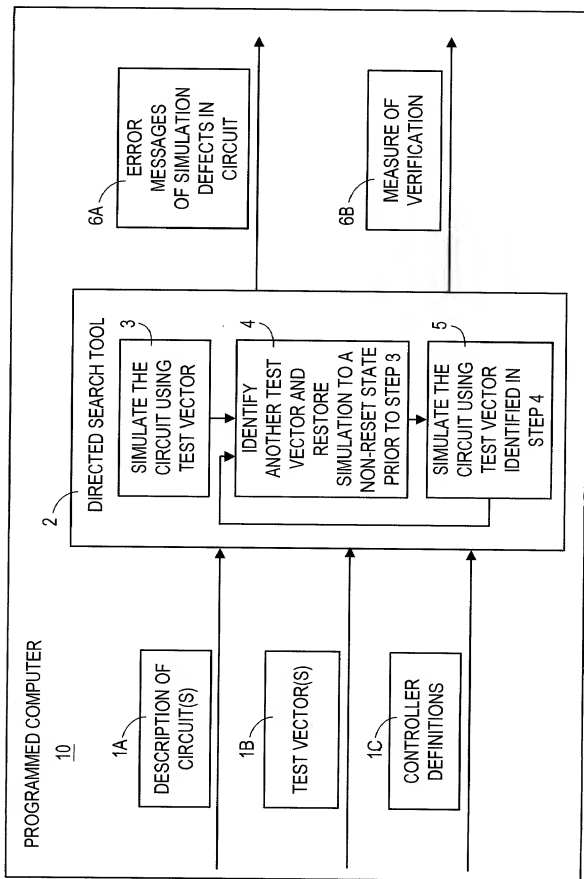


Fig. 1A

FIG. 1A

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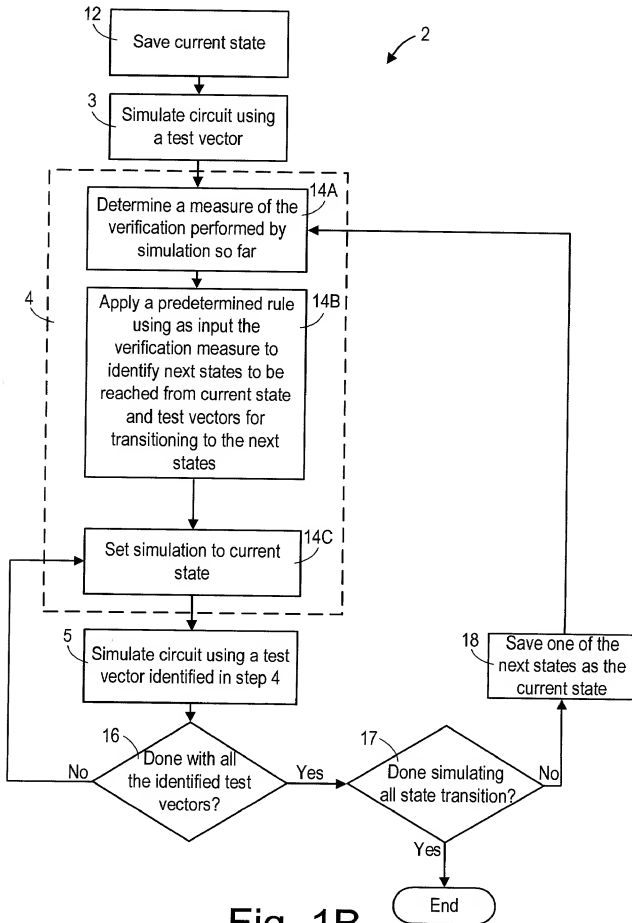


Fig. 1B

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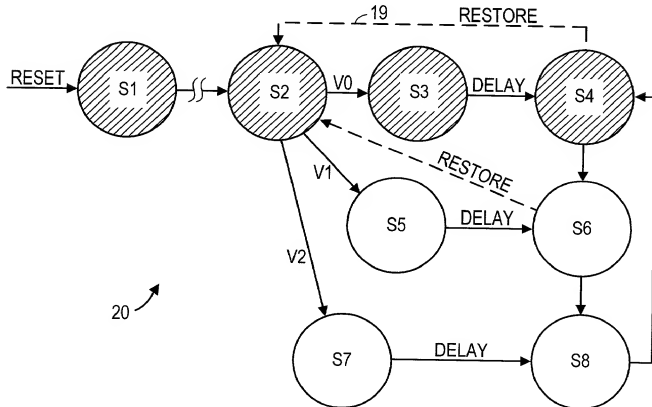


Fig. 1C

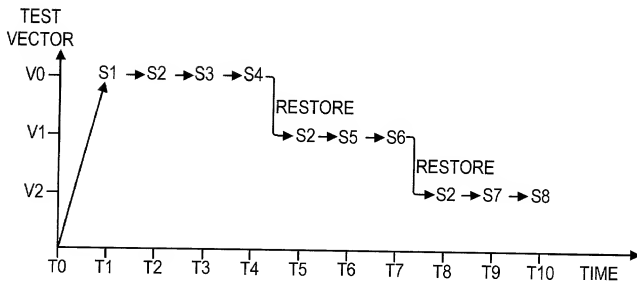
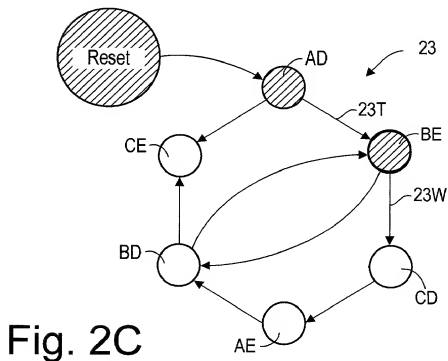
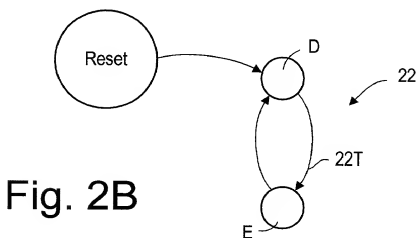
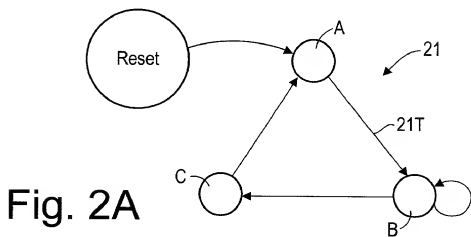


Fig. 1D

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106120-50064860

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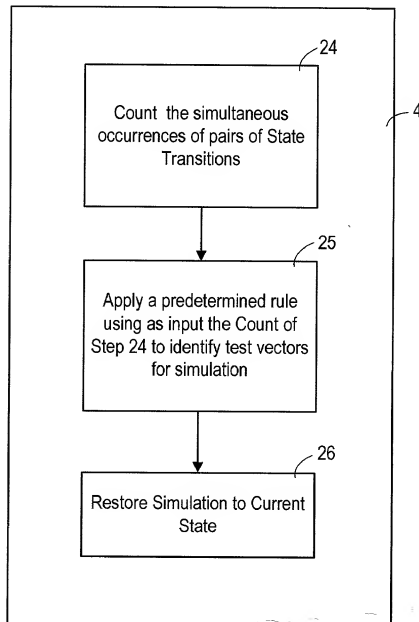


Fig. 2D

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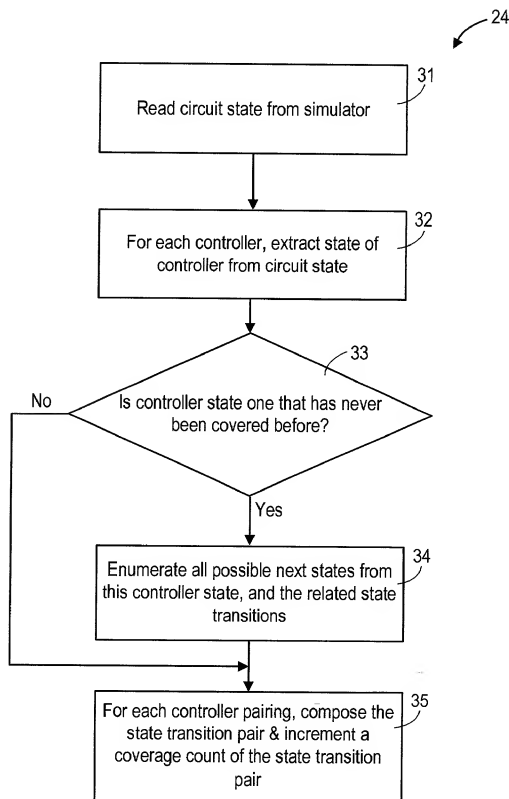


Fig. 2E

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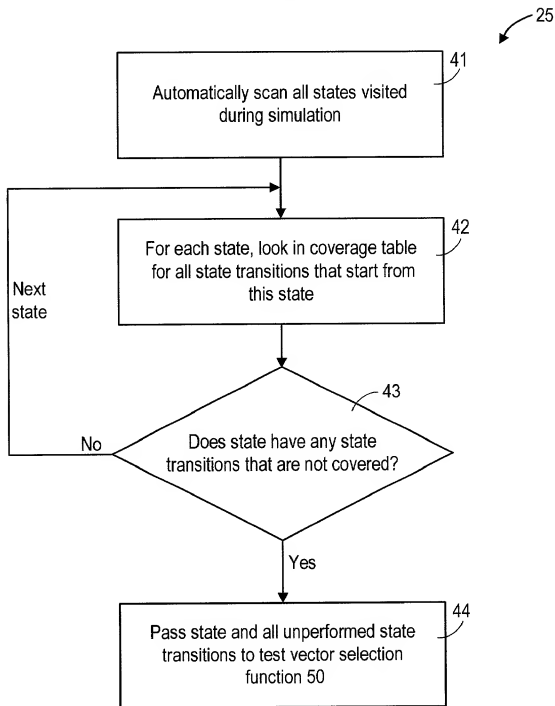


Fig. 2F

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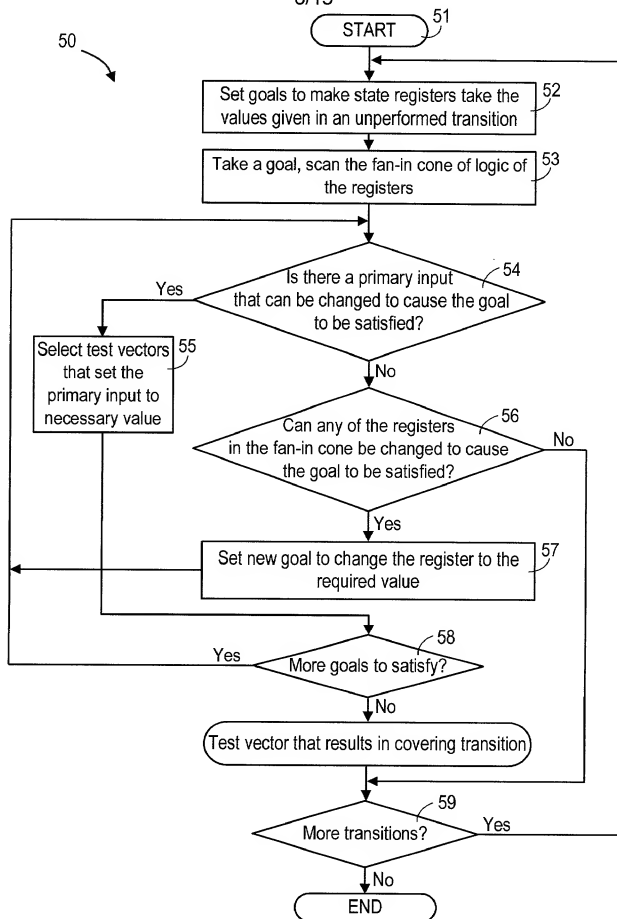


Fig. 2G

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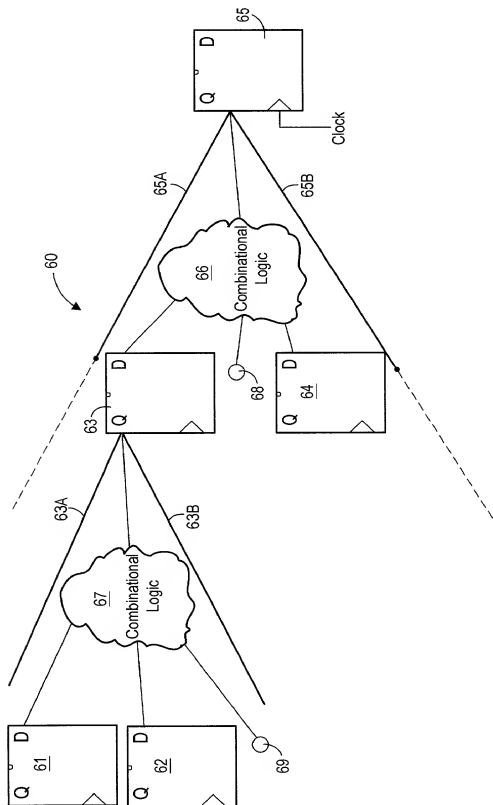


Fig. 2H

FIG. 2H

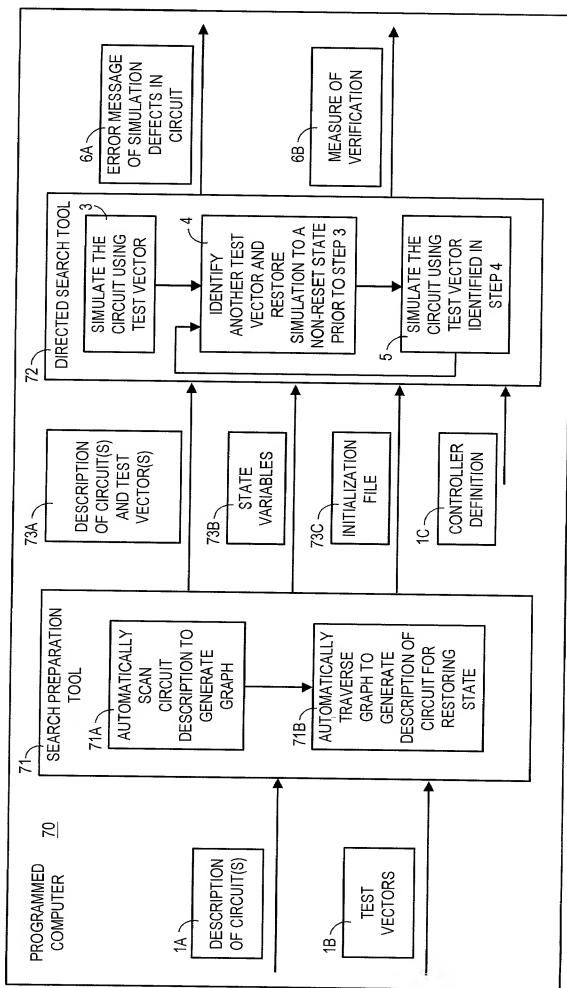


Fig. 3A

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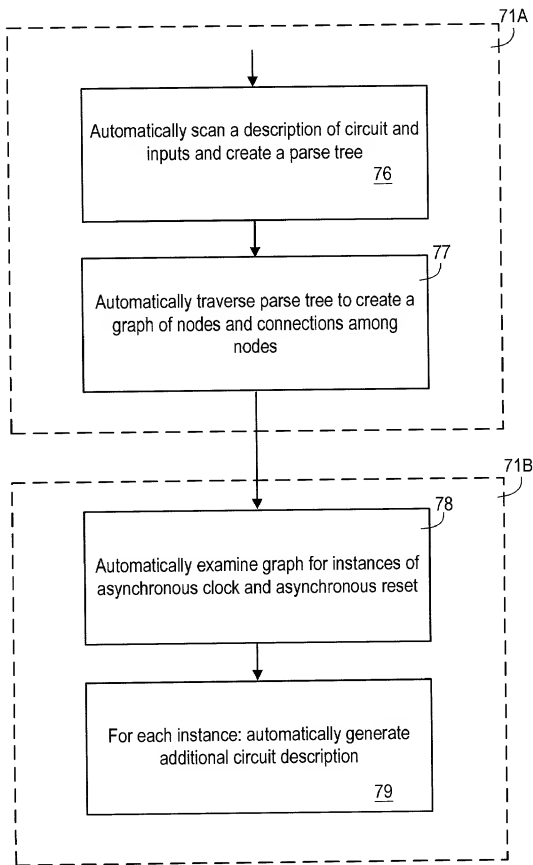


Fig. 3B

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Fig. 3C

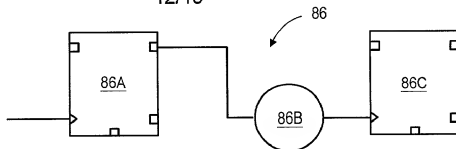


Fig. 3D

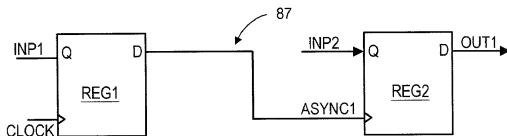


Fig. 3E

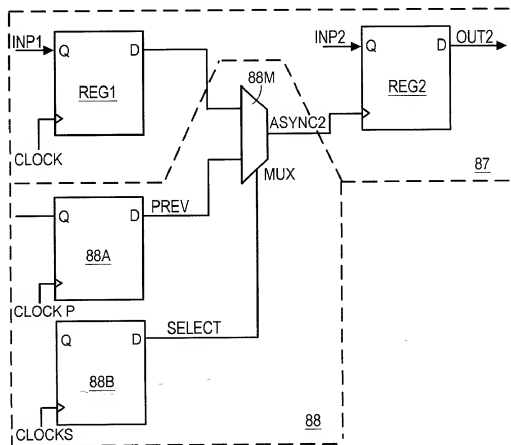
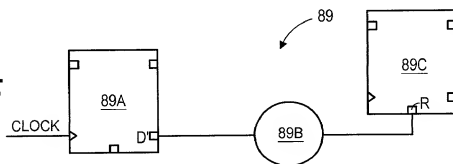


Fig. 3F



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4

Write into at least a majority of storage elements of the circuit the values held in Current State

81

Force each "Previous Value Register " to hold the value of first storage element in state prior to Current State

82

Force each "Asynchronous Mux Select Register" to the value that causes "Mux" to select its input from the "Previous Value Register"

83

Force the simulation to proceed for a non-zero time period.
(Time period is a small fraction of the simulation cycle period).

84

Force each "Asynchronous Mux Select Register" to the value that causes "Mux" to select its input from first storage element

85

Fig. 3G

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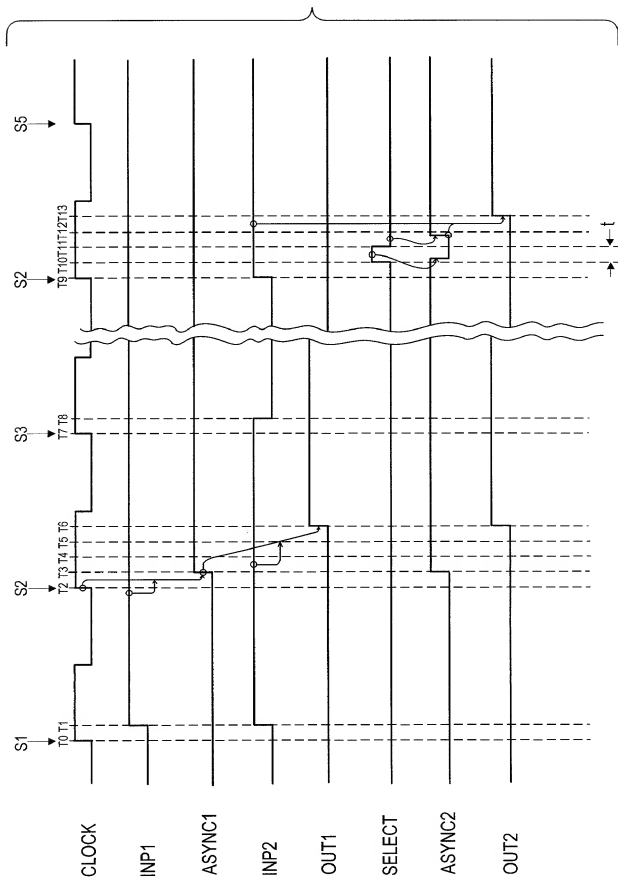


Fig. 3H

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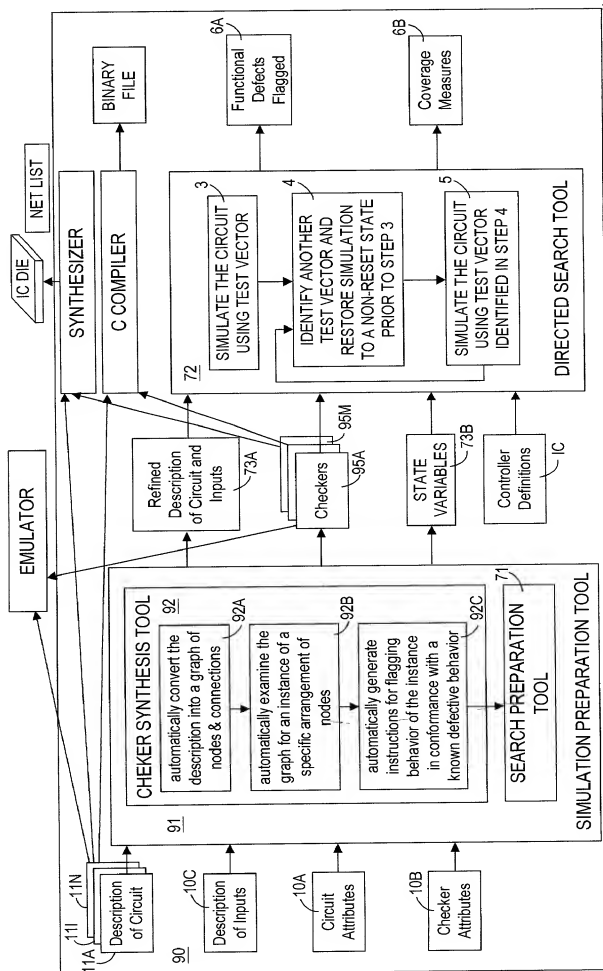


Fig. 4